Sajel Behari

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EDUCATION

The Pennsylvania State University — **University Park, PA**
Penn State College of Engineering — **August 2021 - May 2025**
Bachelor of Science, Computer Engineering — Dean's List Recipient: 2x

RELEVANT EXPERIENCE

OpenDrives — **Remote - Culver City, CA**
Software Engineer and Lead Market Software Developer — **July 2025 – Present**
- Lead frontend development with TS, JS, Node.js, Vue.js, crafting engaging lead magnets and UI web components to boost marketing conversions and webflow.
- Collaborate with teams to design scalable, user-focused solutions, components, and implementations, integrating feedback for continuous improvement.

Kunai - Kun.AI — **Hybrid - Oakland, CA**
Software Engineering Intern — **June 2024 – September 2024**
- Built web components using JavaScript, TypeScript, TailwindCSS, Node.js, and Qwik for high-performance applications with cross-functional teams and Capital One to integrate feedback and drive milestones.

Canova (Startup) — **Hybrid - New Brunswick, NJ**
Software Engineer — **August 2025 – Present**
- Develop object-oriented TypeScript and Python backend systems for real-time data processing in a mobile app.
- Build responsive UI components, integrating APIs for interactive, cross-platform user experiences.

VoteU - VoteU.AI — **Remote**
Sole Full Stack Developer — ***October* 2024**
- Developed a web app to boost civic engagement using React, Node.js, TypeScript, Python, Flask, and Firebase.
- Integrated OpenAI API for an AI-driven chatbot providing localized voter information to a responsive UI.

KEY SKILLS

- Verilog, C, Python, Java, JavaScript, TypeScript, C++, HTML, TailwindCSS, AutoCAD, SolidWorks, React, Qwik, Next.js, Node.js, Flask, Microsoft Azure, MongoDB, XGBoost, Prophet, Pandas, Selenium
- Leadership, Public Speaking, Team Building, Strategizing, Presentation, Agile, Scrum

PROJECTS

CORDIC-Based Signal Processor
- Designed a signal processor in Vitis HLS for a Zedboard FPGA, integrating a 25-tap complex FIR filter and CORDIC rotator to compute signal magnitude and phase, using hls::stream for dataflow.
- Optimized with ap_fixed<16,8> fixed-point arithmetic to support -50 to +50 range, reducing DSP usage by 25% while maintaining 0.2 precision, and applied DATAFLOW pragma to enable concurrent processing.

Autonomous Two-Axis Solar Tracker - 3rd Place in Best Poster for LF Capstone Showcase
- Developed an Arduino-based solar tracker using custom algorithms for solar elevation and azimuth, integrating A4988 Driver, IMU Breakout, and DS3231 RTC for precise, autonomous operation without WiFi.
- Engineered a one-actuator mechanism achieving both daily azimuth and seasonal elevation tracking to maximize solar energy capture.

CPU
- Implemented a mini CPU using Verilog and MIPS in the Vivado IDE, applying advanced computer architecture and digital design concepts.
- Developed a datapath architecture with integrated pipelining for instruction execution and memory allocation. Used FPGA design and format, Verilog programming, and CPU architecture.